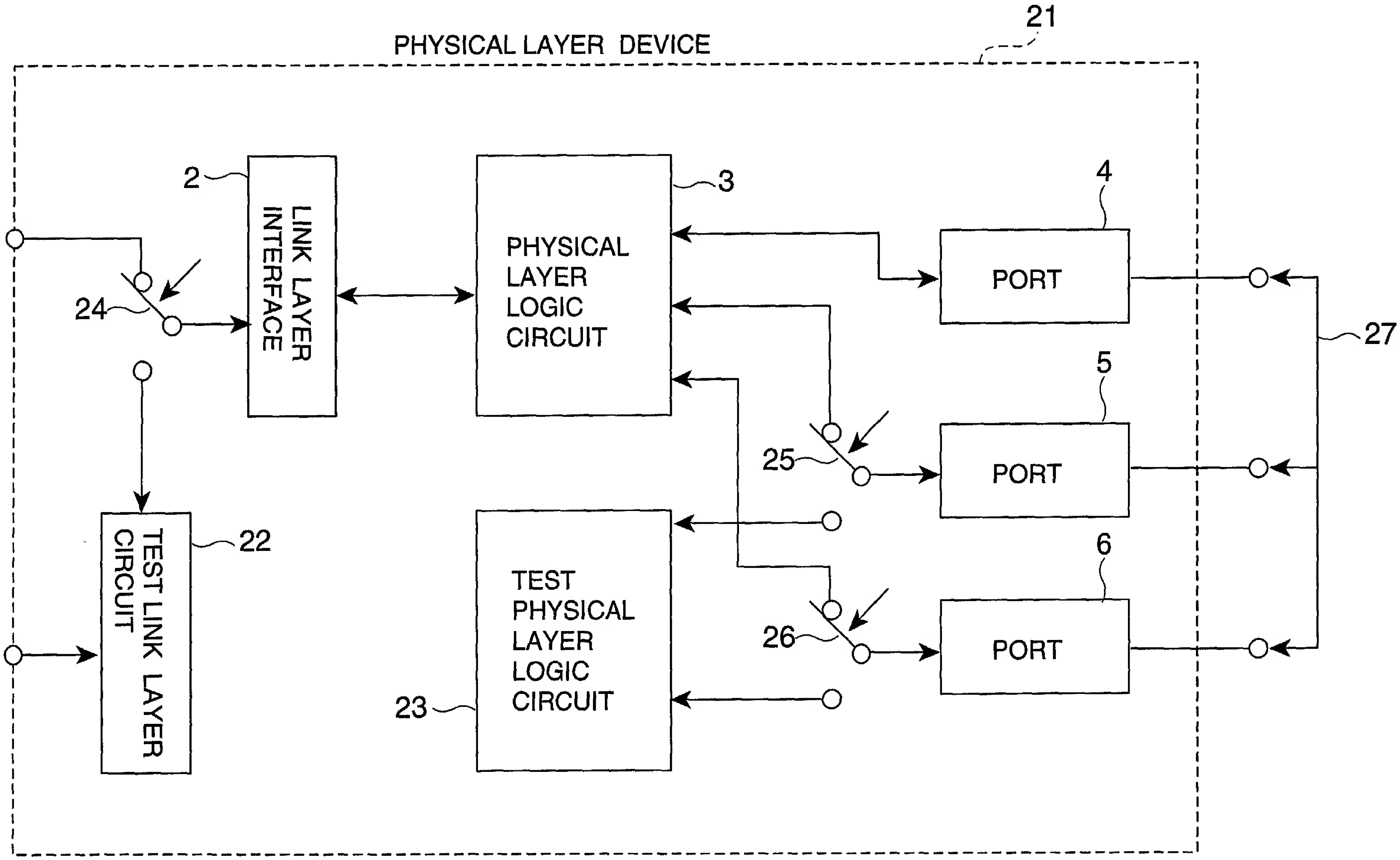
PHYSICAL LAYER DEVICE
21
2
LINK LAYER INTERFACE
3
PHYSICAL LAYER LOGIC CIRCUIT
4
PORT
5
PORT
6
PORT
27
24
25
26
22
TEST LINK LAYER CIRCUIT
23
TEST PHYSICAL LAYER LOGIC CIRCUIT

FIG. 1

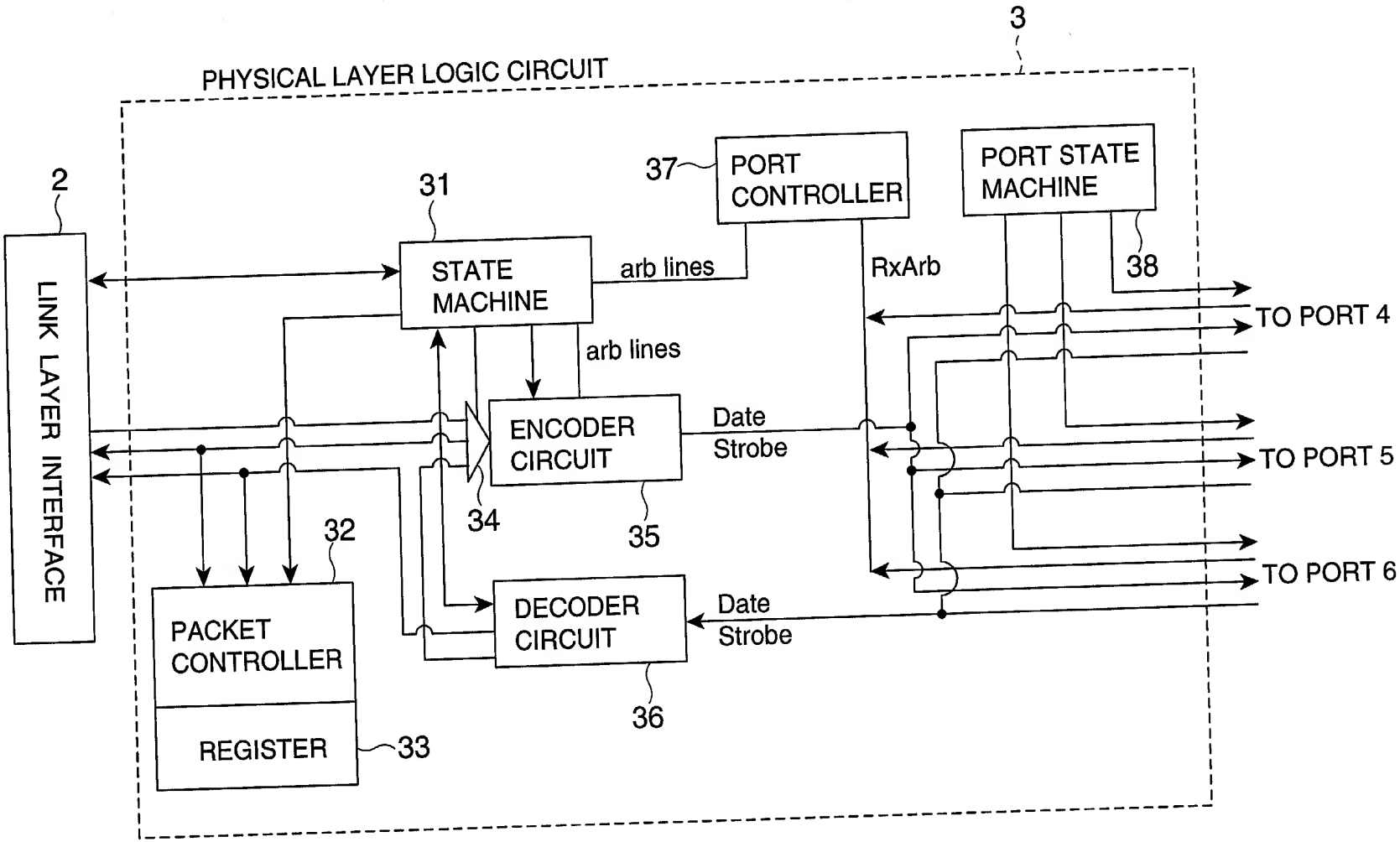

FIG. 2

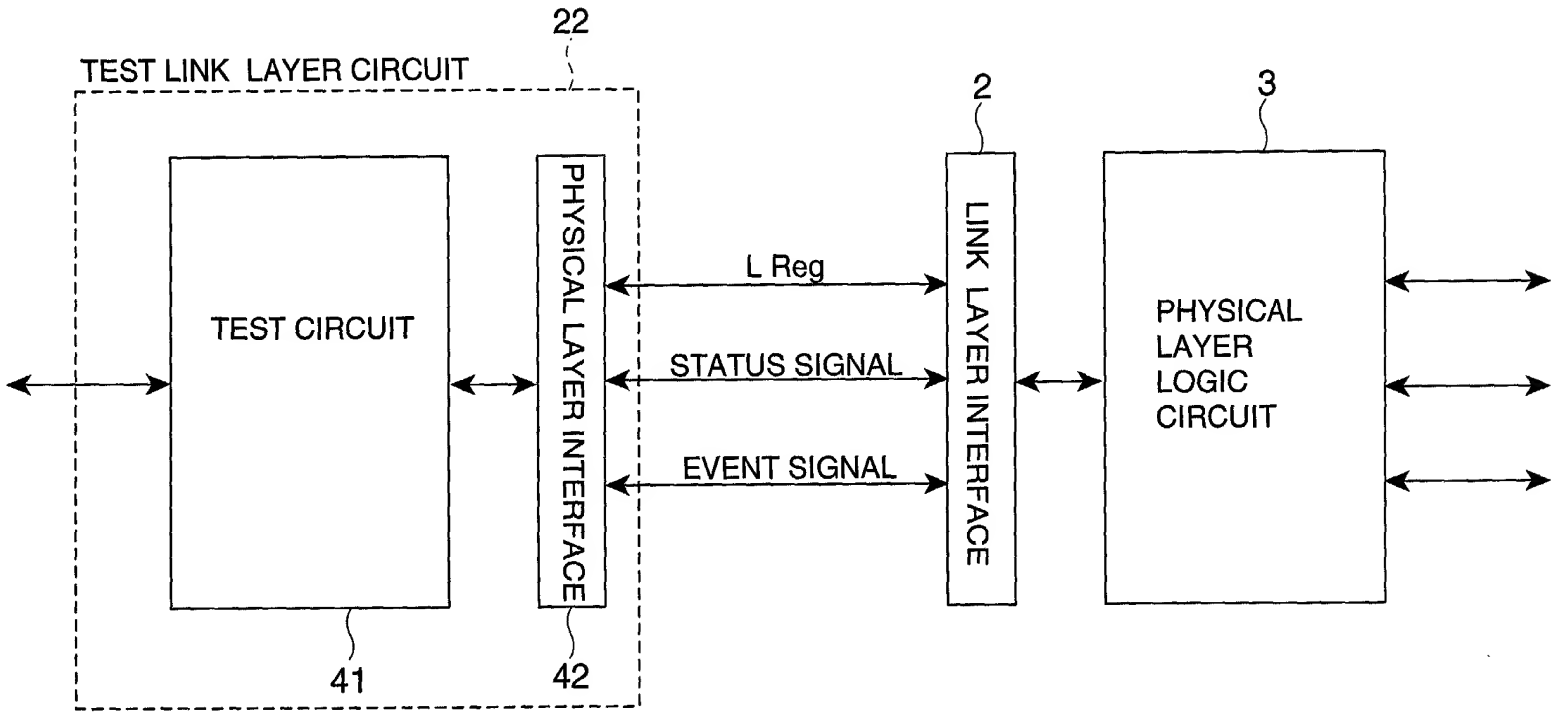

FIG. 3

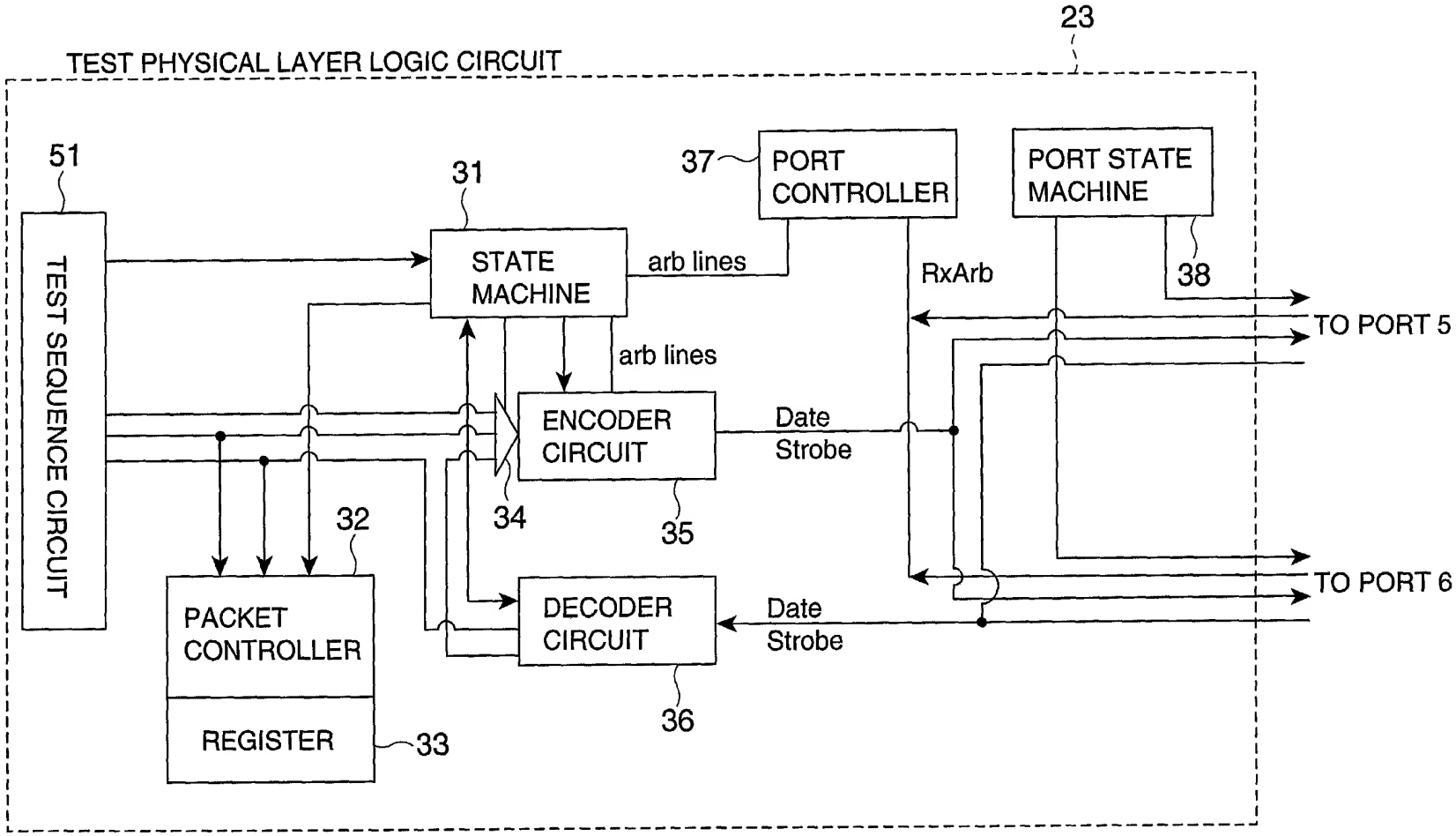

FIG. 4

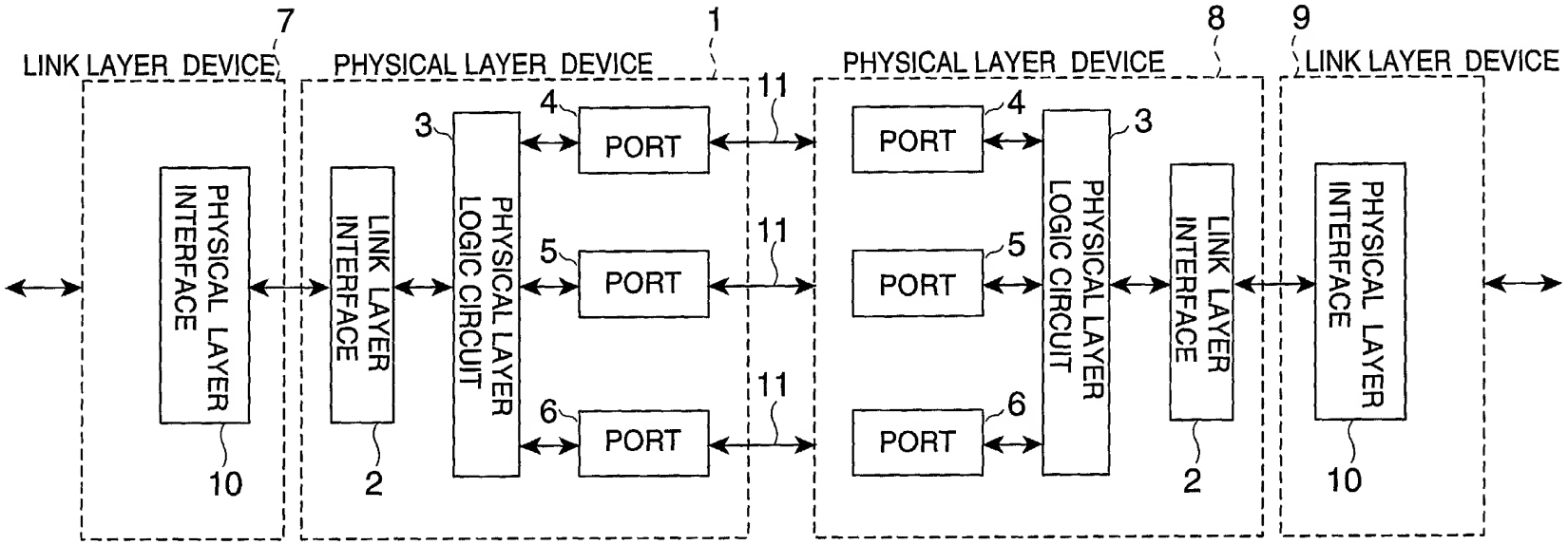

FIG. 5

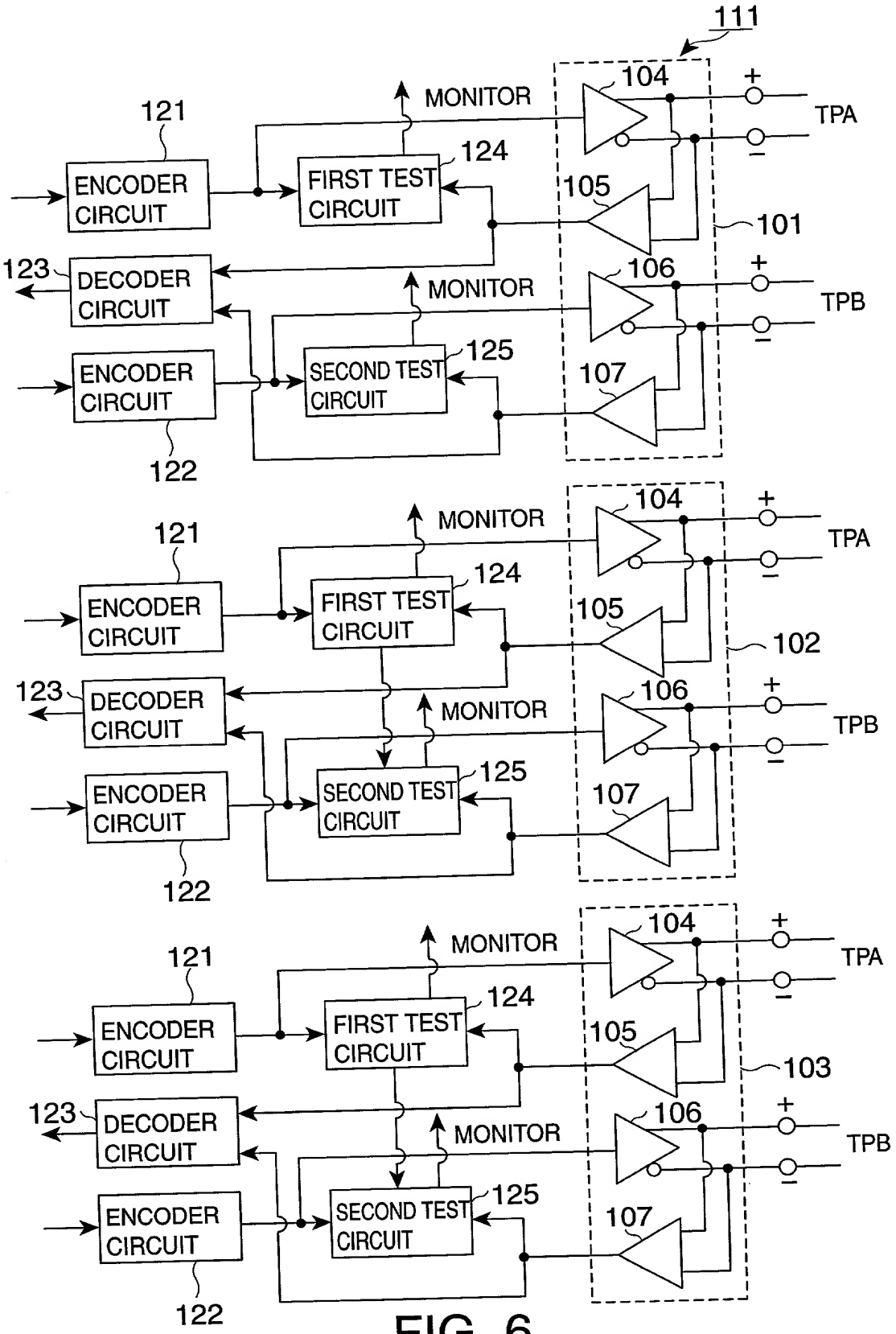

FIG. 6

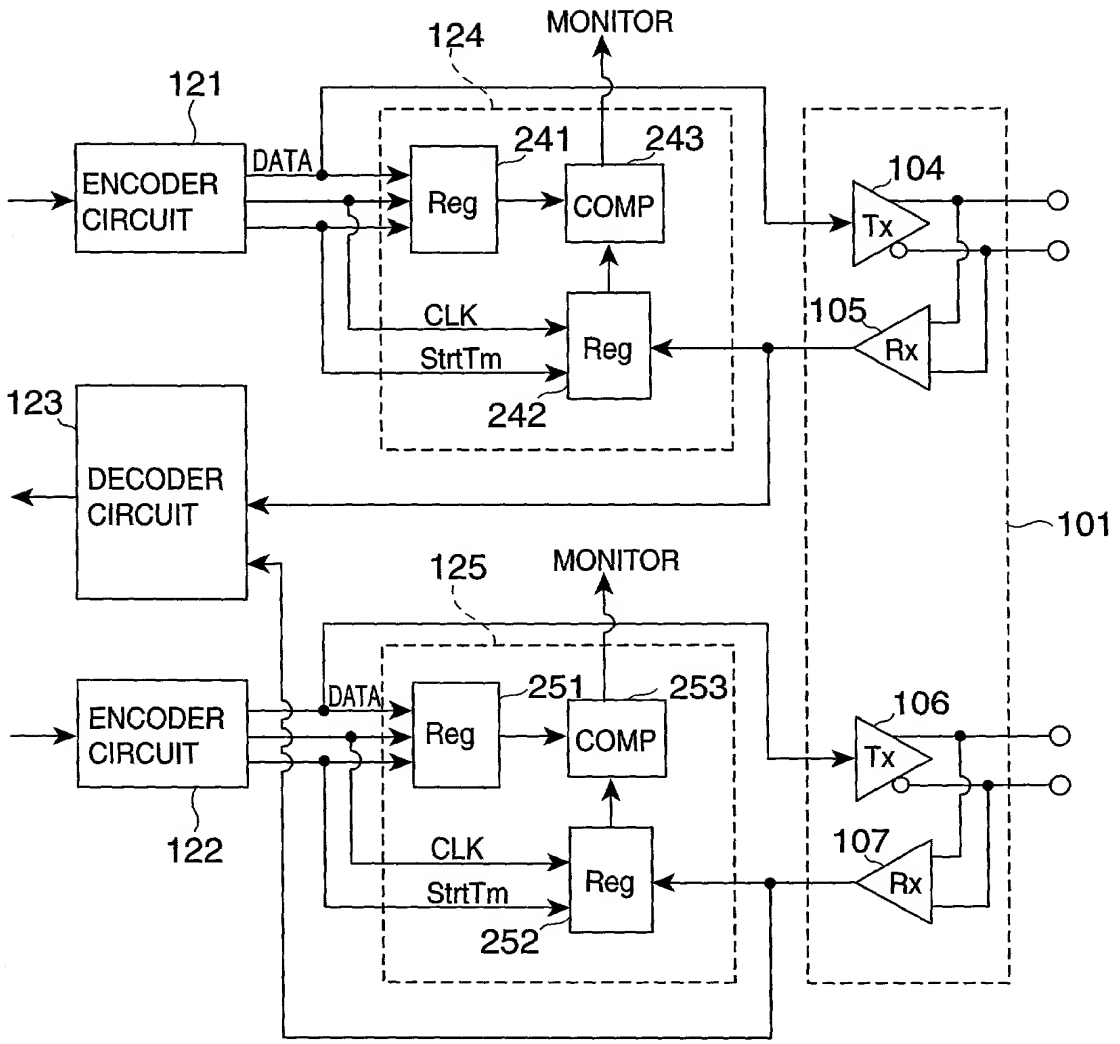
124
MONITOR
121
ENCODER CIRCUIT
DATA
241
243
Reg
COMP
104
Tx
CLK
StrtTm
Reg
105
Rx
242
123
DECODER CIRCUIT
101
125
MONITOR
ENCODER CIRCUIT
DATA
251
253
Reg
COMP
106
Tx
122
CLK
StrtTm
Reg
107
Rx
252

FIG. 7

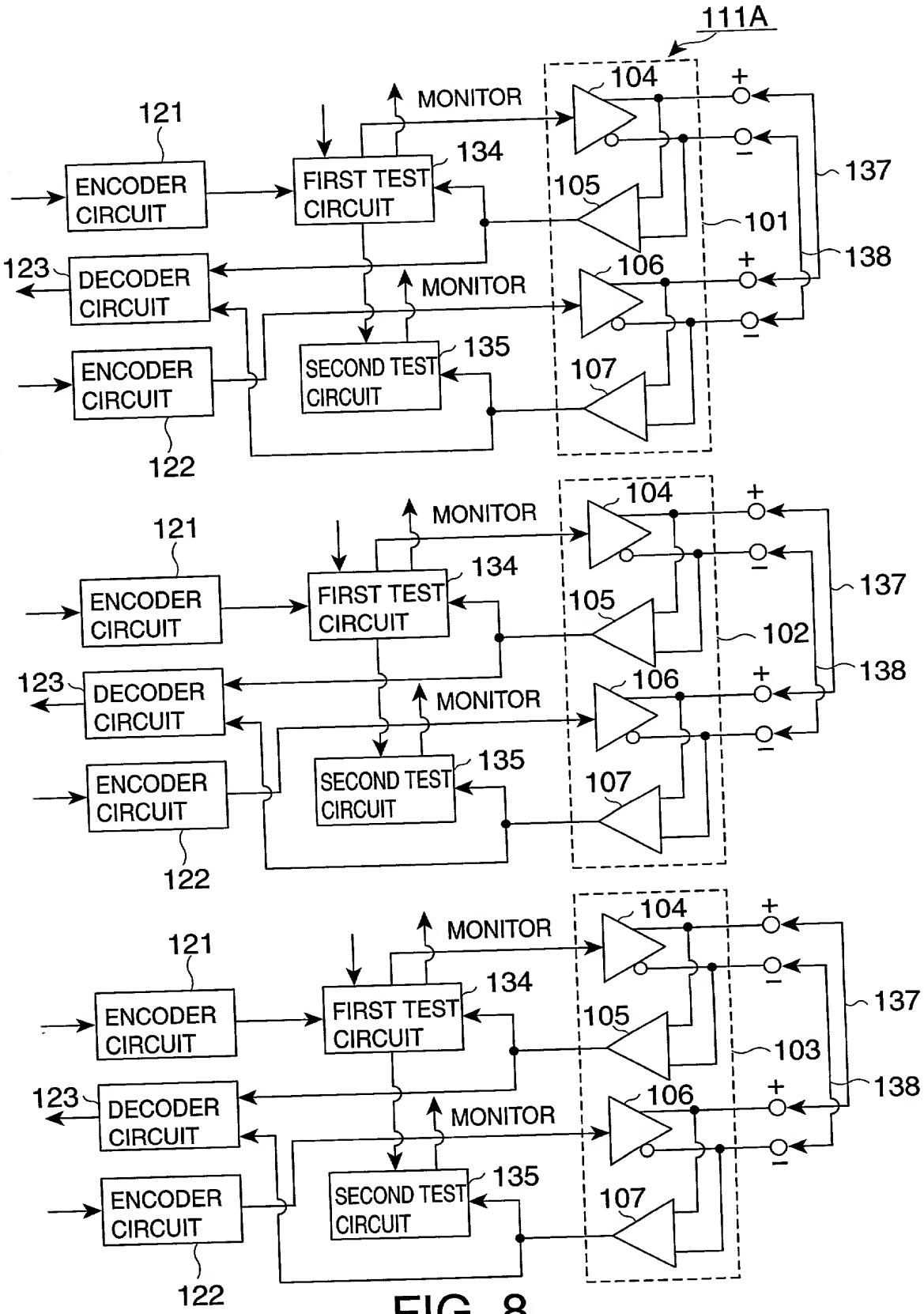
111A
121
ENCODER CIRCUIT
FIRST TEST CIRCUIT
134
MONITOR
104
105
101
137
138
123
DECODER CIRCUIT
106
MONITOR
ENCODER CIRCUIT
SECOND TEST CIRCUIT
135
107
122
121
ENCODER CIRCUIT
FIRST TEST CIRCUIT
134
MONITOR
104
105
102
137
138
123
DECODER CIRCUIT
106
MONITOR
ENCODER CIRCUIT
SECOND TEST CIRCUIT
135
107
122
121
ENCODER CIRCUIT
FIRST TEST CIRCUIT
134
MONITOR
104
105
103
137
138
123
DECODER CIRCUIT
106
MONITOR
ENCODER CIRCUIT
SECOND TEST CIRCUIT
135
107
122

FIG. 8

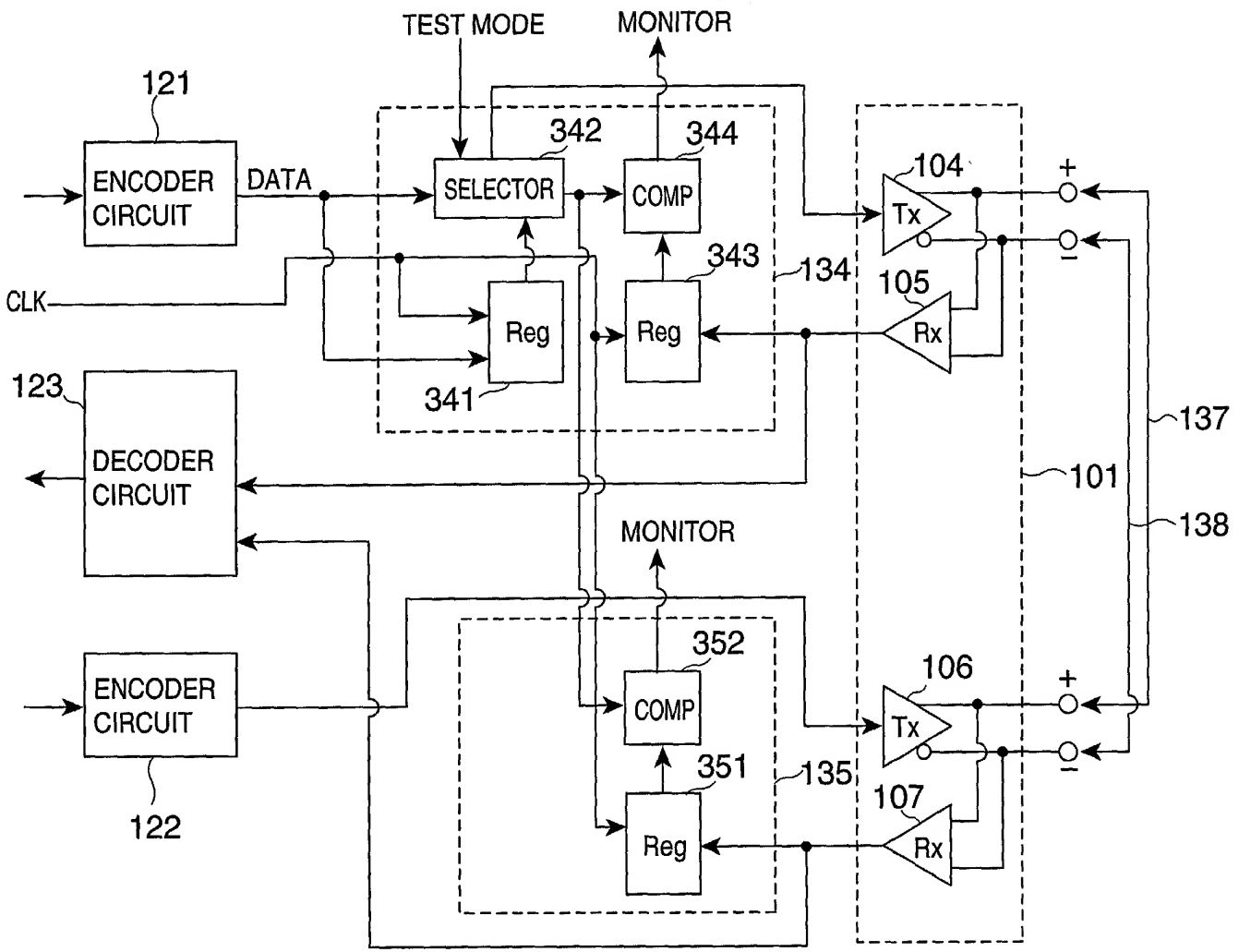

FIG. 9

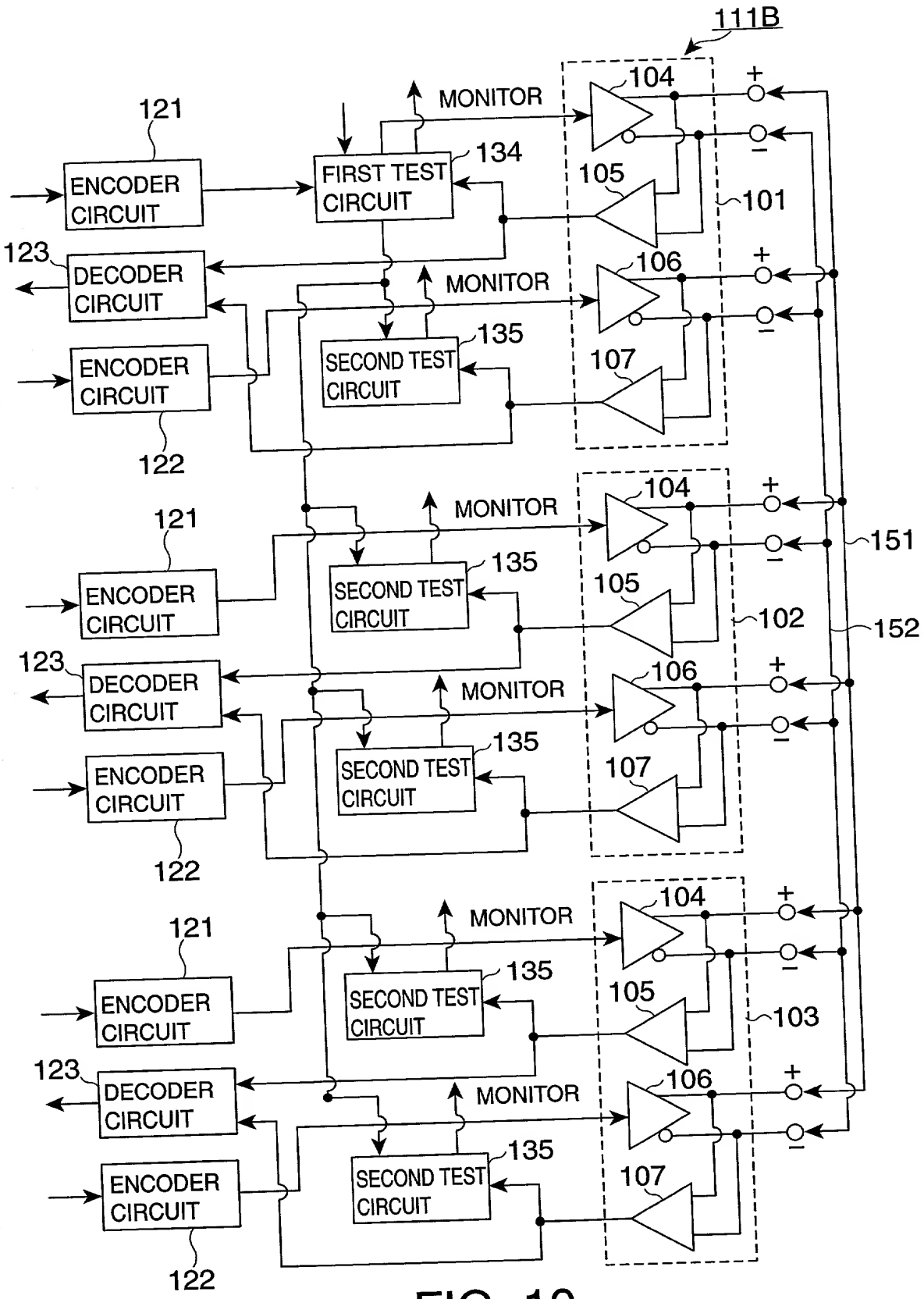
111B
121
ENCODER CIRCUIT
FIRST TEST CIRCUIT
134
MONITOR
104
105
101
123
DECODER CIRCUIT
106
MONITOR
ENCODER CIRCUIT
135
SECOND TEST CIRCUIT
107
122
121
ENCODER CIRCUIT
MONITOR
104
151
135
SECOND TEST CIRCUIT
105
102
152
123
DECODER CIRCUIT
106
MONITOR
ENCODER CIRCUIT
135
SECOND TEST CIRCUIT
107
122
121
ENCODER CIRCUIT
MONITOR
104
135
SECOND TEST CIRCUIT
105
103
123
DECODER CIRCUIT
106
MONITOR
ENCODER CIRCUIT
135
SECOND TEST CIRCUIT
107
122

FIG. 10

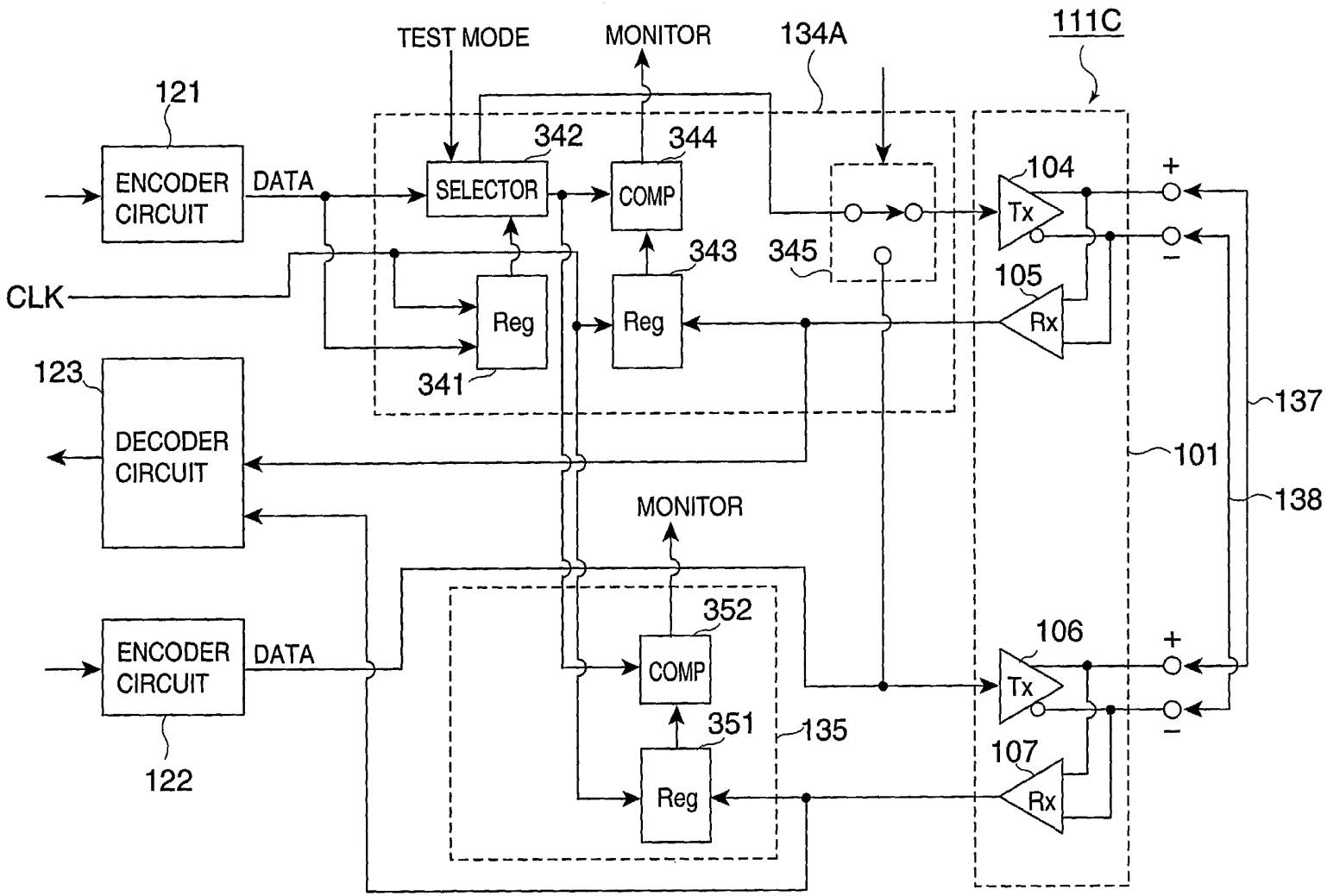

FIG. 11

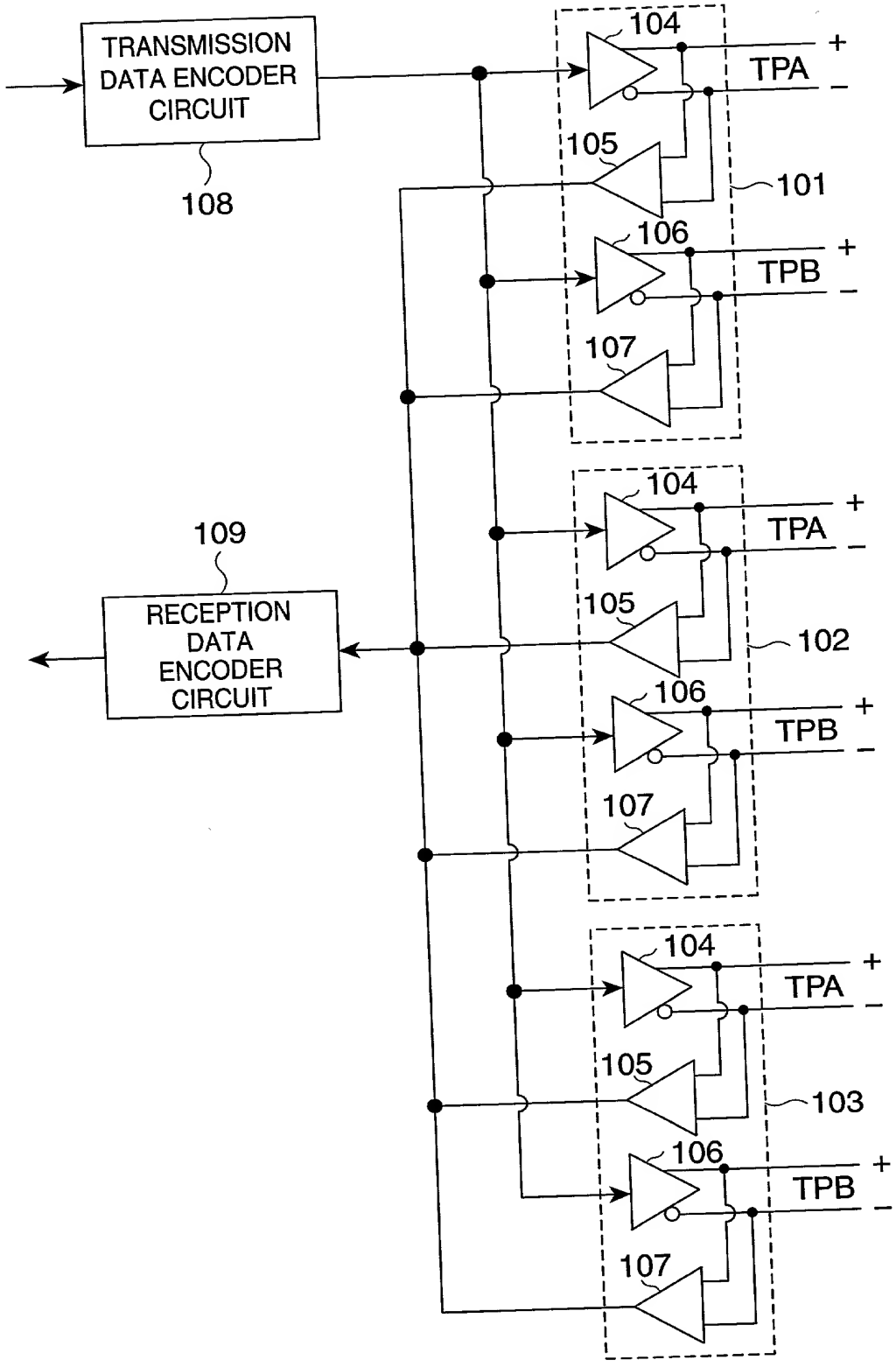
TRANSMISSION DATA ENCODER CIRCUIT
108
109
RECEPTION DATA ENCODER CIRCUIT
104
105
106
107
TPA
TPB
+
–
101
102
103

FIG. 12